


EXHIBIT 012

U.S. Patent No. 8,086,800 (Radulescu and Goossens)

“Integrated circuit and method for buffering to optimize burst length in networks on chips”

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
<p>10. A method for buffering data in an integrated circuit having a plurality of processing modules being connected with an interconnect through interface units, wherein a first processing module communicates to a second processing module using transactions, the method comprising the acts of:</p>	<p>Without conceding that the preamble of claim 10 of the '800 Patent is limiting, Qualcomm Incorporated and Qualcomm Technologies, Inc.'s (together, “Qualcomm”) Snapdragon 8+ Gen 1 Mobile Platform (hereinafter, the “Snapdragon SoC”) is an integrated circuit and performs a method for buffering data in an integrated circuit having a plurality of processing modules being connected with an interconnect through interface units, wherein a first processing module communicates to a second processing module using transactions), either literally or under the doctrine of equivalents.</p> <div data-bbox="510 573 636 695">  </div> <h2 data-bbox="661 609 1606 662">Snapdragon 8+ Gen 1 Mobile Platform</h2> <p data-bbox="510 885 1728 950">New power and performance enhancements deliver the ultimate boost across all your on-device experiences.</p> <p data-bbox="510 1015 1707 1201">The Snapdragon® 8+ Gen 1 Mobile Platform is our premium-tier powerhouse. Qualcomm® Adreno™ GPU offers a 10% increase in GPU clock speeds and 30% GPU power reduction while the Qualcomm® Kryo™ CPU provides 10% better CPU performance and 30% CPU improved power efficiency. Plus, this platform delivers additional power savings and extended performance across the board—including over 80 minutes longer video streaming and more than 50 minutes longer web browsing.</p>

¹ The Snapdragon SoC is charted as a representative product made used, sold, offered for sale, and/or imported by or on behalf of Qualcomm. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein.


U.S. Patent No. 8,086,800 (Radulescu and Goossens)

“Integrated circuit and method for buffering to optimize burst length in networks on chips”

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p data-bbox="499 250 1877 326">https://www.qualcomm.com/products/application/smartphones/snapdragon-8-series-mobile-platforms/snapdragon-8-plus-gen-1-mobile-platform</p> <p data-bbox="499 407 1787 521">The Snapdragon SoC comprises a plurality of processing modules, for example Qualcomm Adreno GPU; Qualcomm Kryo CPU; Qualcomm Hexagon Processor; and Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU):</p>

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<div data-bbox="506 253 898 386">  <p>Snapdragon 8+ mobile platform Gen 1</p> </div> <div data-bbox="1457 277 1732 298">SPECIFICATIONS & FEATURES</div> <div data-bbox="506 448 714 472"> <p>Artificial Intelligence</p> <hr/> <p>Qualcomm® Adreno™ GPU</p> <hr/> <p>Qualcomm® Kryo™ CPU</p> <hr/> <p>Qualcomm® Hexagon™ Processor</p> <ul style="list-style-type: none"> • Fused AI Accelerator <ul style="list-style-type: none"> • Hexagon Tensor Accelerator • Hexagon Vector eXtensions • Hexagon Scalar Accelerator • Support for mix precision (INT8+INT16) • Support for all precisions (INT8, INT16, FP16) <hr/> <p>Qualcomm® Sensing Hub</p> <hr/> <p>5G Modem-RF System</p> <hr/> <p>Snapdragon® X65 5G Modem-RF System</p> <ul style="list-style-type: none"> • 5G mmWave and sub-6 GHz, standalone • (SA) and non-standalone (NSA) modes, FDD, TDD • Dynamic Spectrum Sharing • mmWave: 8 carriers, 2x2 MIMO • Sub-6 GHz: 4x4 MIMO • Qualcomm® 5G PowerSave 2.0 • Qualcomm® Smart Transmit™ 2.0 technology • Qualcomm® Wideband Envelope Tracking • Qualcomm® AI-Enhanced Signal Boost • Global 5G multi-SIM <hr/> <p>Downlink: Up to 10 Gbps</p> <hr/> <p>Multimode support: 5G NR, LTE including CBRS, WCDMA, HSPA, CDMA 1x, EV-DO, GSM/EDGE</p> <hr/> </div> <div data-bbox="932 448 1012 472"> <p>Camera</p> <hr/> <p>Qualcomm Spectra™ Image Signal Processor</p> <ul style="list-style-type: none"> • Triple 18-bit ISPs • Up to 3.2 Gigapixels per Second computer vision ISP (CV-ISP) • Up to 36 MP triple camera @ 30 FPS with Zero Shutter Lag • Up to 64+36 MP dual camera @ 30 FPS with Zero Shutter Lag • Up to 108 MP single camera @ 30 FPS with Zero Shutter Lag • Up to 200 Megapixel Photo Capture <hr/> <p>Rec. 2020 color gamut photo and video capture</p> <hr/> <p>Up to 10-bit color depth photo and video capture</p> <hr/> <p>8K HDR Video Capture + 64 MP Photo Capture</p> <hr/> <p>10-bit HEIF: HEIC photo capture, HEVC video capture</p> <hr/> <p>Video Capture Formats: HDR10+, HDR10, HLG, Dolby Vision</p> <hr/> <p>8K HDR Video Capture @ 30 FPS</p> <hr/> <p>4K Video Capture @ 120 FPS</p> <hr/> <p>Slow-mo video capture at 720p @ 960 FPS</p> <hr/> <p>Bokeh Engine for Video Capture</p> <hr/> <p>Video super resolution</p> <hr/> <p>Multi-frame Noise Reduction (MFNR)</p> <hr/> <p>Locally Motion Compensated Temporal Filtering</p> <hr/> <p>Multi-Frame and triple exposure staggered/digital overlap HDR dual-sensor support</p> <hr/> <p>AI-based face detection, auto-focus, and auto-exposure</p> <hr/> </div> <div data-bbox="1352 448 1398 472"> <p>CPU</p> <hr/> <p>Kryo CPU</p> <ul style="list-style-type: none"> • Up to 3.2 GHz, with Arm Cortex-X2 technology • 64-bit Architecture <hr/> <p>Visual Subsystem</p> <hr/> <p>Adreno GPU</p> <ul style="list-style-type: none"> • Vulkan® 1.1 API support • HDR gaming (10-bit color depth, Rec. 2020 color gamut) • Physically Based Rendering • Volumetric Rendering • Adreno Frame Motion Engine • API Support: OpenGL® ES 3.2, OpenCL™ 2.0 FP, Vulkan 1.1 • Hardware-accelerated H.265 and VP9 decoder • HDR Playback Codec support for HDR10+, HDR10, HLG and Dolby Vision <hr/> <p>Security</p> <hr/> <p>Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU)</p> <hr/> <p>Trust Management Engine</p> <hr/> <p>Qualcomm® wireless edge services (WES) and premium security features</p> <hr/> <p>Qualcomm® 3D Sonic Sensor and Qualcomm® 3D Sonic Max (fingerprint sensor)</p> <hr/> <p>Qualcomm® Type-1 Hypervisor</p> <hr/> </div>

U.S. Patent No. 8,086,800 (Radulescu and Goossens)

“Integrated circuit and method for buffering to optimize burst length in networks on chips”


'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<div data-bbox="506 245 892 743"> <p>Wi-Fi & Bluetooth*</p> <p>Qualcomm* FastConnect™ 6900 System</p> <ul style="list-style-type: none"> • Wi-Fi Standards: Wi-Fi 6E, Wi-Fi 6 (802.11ax), • Wi-Fi 5 (802.11ac), 802.11a/b/g/n • Wi-Fi Spectral Bands: 24 GHz, 5 GHz, 6 GHz • Peak speed: 3.6 Gbps • Channel Bandwidth: 20/40/80/160 MHz • 8-stream sounding (for 8x8 MU-MIMO) • MIMO Configuration: 2x2 (2-stream) • MU-MIMO (Uplink & Downlink) • 4K QAM • OFDMA (Uplink & Downlink) • 4-Stream (2x2 + 2x2) Dual Band Simultaneous (DBS) • Wi-Fi Security: WPA3-Enterprise, WPA3- Enhanced Open, WPA3 Easy Connect, WPA3-Personal <p>Integrated Bluetooth</p> <ul style="list-style-type: none"> • Bluetooth Features: Bluetooth* 5.3, LE Audio, Dual Bluetooth antennas • Bluetooth audio: Snapdragon Sound™ Technology with support for Qualcomm* aptX™ Voice, aptX Lossless, aptX Adaptive, and LE audio </div> <div data-bbox="506 797 676 821"> <p>snapdragon.com</p> </div> <div data-bbox="506 854 1745 1002"> <p><small>*Snapdragon 8+ Gen 1 Mobile Platform also available in 3 GHz CPU version. Maximum CPU speed will vary based on platform version. Consult OEM specifications for device CPU speed. Certain optional features available subject to Carrier and OEM selection for an additional fee.</small></p> <p><small>Snapdragon, Qualcomm, Qualcomm Hexagon, Qualcomm 5G PowerSave, Qualcomm Kryo, Qualcomm Smart Transmit, Qualcomm Wideband Envelope Tracking, Qualcomm AI-Enhanced Signal Boost, Qualcomm Spectra, Qualcomm Adreno, Qualcomm 3D Sonic Sensor, Qualcomm Type-T Hypervisor, Qualcomm Adreno, Qualcomm Sensing Hub, Qualcomm 3D Sonic Max, Qualcomm FastConnect, Snapdragon Sound, Qualcomm aptX, Snapdragon Elite Gaming, and Qualcomm Quick Charge are products of Qualcomm Technologies, Inc. and/or its subsidiaries. Qualcomm wireless edge services are offered by Qualcomm Technologies Inc. and/or its subsidiaries.</small></p> <p><small>Snapdragon, Qualcomm, Hexagon, Snapdragon Elite Gaming, Adreno, FastConnect, Snapdragon Sound, Kryo, Smart Transmit, Qualcomm Spectra, Qualcomm Adreno, Snapdragon Sight, and Quick Charge are trademarks or registered trademarks of Qualcomm Incorporated. aptX is a trademark or registered trademark of Qualcomm Technologies International, Ltd.</small></p> <p><small>©2022 Qualcomm Technologies, Inc. and/or its affiliated companies. All Rights Reserved.</small></p> </div> <div data-bbox="506 1044 1461 1118"> <p>https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/Snapdragon-8-plus-Gen-1-Product-Brief.pdf</p> </div> <div data-bbox="506 1161 1858 1278"> <p>The Snapdragon SoC utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the “Arteris NoC”) as an interconnect to connect the plurality of processing modules through interface units:</p> </div> <div data-bbox="919 276 989 302"> <p>Audio</p> </div> <div data-bbox="919 308 1308 451"> <p>Qualcomm Aqstic™ audio codec (WCD9385)</p> <p>New Qualcomm Aqstic smart speaker amplifier (WSA8835)</p> <p>Total Harmonic Distortion + Noise (THD+N), Playback: -108dB</p> <p>Qualcomm* Audio and Voice Communication Suite</p> </div> <div data-bbox="919 475 1005 503"> <p>Display</p> </div> <div data-bbox="919 506 1308 709"> <p>On-Device Display Support:</p> <ul style="list-style-type: none"> • 4K @ 60 Hz • QHD+ @ 144 Hz <p>Maximum External Display Support: up to 4K @ 60 Hz</p> <ul style="list-style-type: none"> • 10-bit color depth, Rec. 2020 color gamut • HDR10 and HDR10+ <p>Demura and subpixel rendering for OLED Uniformity</p> </div> <div data-bbox="1333 245 1442 274"> <p>Charging</p> </div> <div data-bbox="1333 279 1728 305"> <p>Qualcomm* Quick Charge™ 5 Technology</p> </div> <div data-bbox="1333 328 1436 354"> <p>Location</p> </div> <div data-bbox="1333 360 1728 522"> <p>GPS, Glonass, BeiDou, Galileo, QZSS, NavIC capable</p> <p>Dual Frequency GNSS (L1/L5)</p> <p>Sensor-Assisted Positioning</p> <ul style="list-style-type: none"> • Urban pedestrian navigation with sidewalk accuracy • Global freeway lane-level vehicle navigation </div> <div data-bbox="1333 552 1432 579"> <p>Memory</p> </div> <div data-bbox="1333 583 1728 636"> <p>Support for LP-DDR5 memory up to 3200 MHz</p> <p>Memory Density: up to 16 GB</p> </div> <div data-bbox="1333 657 1570 685"> <p>General Specifications</p> </div> <div data-bbox="1333 691 1728 797"> <p>Full Suite of Snapdragon Elite Gaming™ features</p> <p>4 nm Process Technology</p> <p>USB Version 3.1; USB Type-C Support</p> <p>Part Number: SM8475</p> </div>

U.S. Patent No. 8,086,800 (Radulescu and Goossens)
“Integrated circuit and method for buffering to optimize burst length in networks on chips”

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<div><p>Qualcomm</p><p></p><p>Arteris-developed NoC technology is the backbone of Snapdragon application processors & LTE modems, Atheros wireless connectivity SoCs, and CSR IoT products.</p><p>LEARN MORE »</p></div> <p>https://web.archive.org/web/20210514110614/https://www.artemis.com/customers</p>

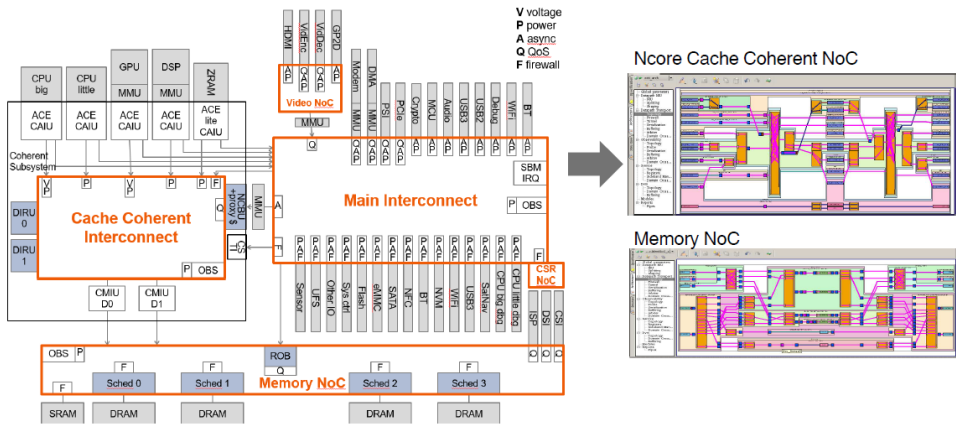
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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p data-bbox="583 248 1495 305" style="text-align: center;">Certain Arteris Technology Assets Acquired</p> <p data-bbox="827 337 1251 370" style="text-align: center;">by Kurt Shuler, on October 31, 2013</p> <p data-bbox="512 415 1373 448">Arteris to continue to license, support and maintain Arteris FlexNoC® interconnect IP</p> <p data-bbox="512 472 1562 597">SUNNYVALE, California — October 31, 2013 — Arteris Inc., a leading innovator and supplier of silicon-proven commercial network-on-chip (NoC) interconnect IP solutions, today announced that Qualcomm Technologies, Inc. (“Qualcomm”), a subsidiary of Qualcomm Incorporated, has acquired certain technology assets from Arteris and hired personnel formerly employed by Arteris.</p> <p data-bbox="512 634 1495 808"> “Arteris NoC technology has been and will continue to be a key enabler for creating larger and more complex chips in a shorter amount of time at a lower cost. This acquisition of our technology assets represents a validation of the value of Arteris’ Network-on-Chip interconnect IP technology. </p> <p data-bbox="1352 857 1516 889" style="text-align: right;">ARTERIS</p> <p data-bbox="1213 943 1516 963" style="text-align: right;"><i>K. Charles Janac, President and CEO, Arteris</i></p> <p data-bbox="512 1019 1528 1208">As part of the acquisition transaction, Arteris retains the right to license, support and maintain the existing Arteris FlexNoC and Arteris FlexLLI product lines in order to fulfill existing and new licensing contracts. Qualcomm has agreed to make certain FlexNoC updates available to Arteris based upon an agreed upon schedule and provide certain engineering support to Arteris. Arteris has rights to make customer support-related modifications to FlexNoC. There are no changes in Arteris’ contractual obligations or operations with customers or industry partners.</p> <p data-bbox="504 1256 1797 1333"> https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31; https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team </p>

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	<p>A large SoC, such as the Snapdragon SoC may include multiple classes of Arteris NoC interconnect:</p> <p>Logical Interconnect Topology Development</p> <p>FLEXNOC & NCORE INTERCONNECT IPS DEFINE ARCHITECTURES</p>  <ul style="list-style-type: none"> • ArChip16 Example: Large SoCs have multiple classes of interconnect <ul style="list-style-type: none"> – Non-coherent, Coherent, Control/Status, Observability, etc. • Ncore & FlexNoC interconnects are managed separately from IP blocks, increasing design flexibility <p>See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.</p> <p>The Arteris NoC is an interconnect connects the plurality of processing modules in the Snapdragon SoC through interface units, wherein a first processing module communicates to a second processing module using transactions.</p>

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	<p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

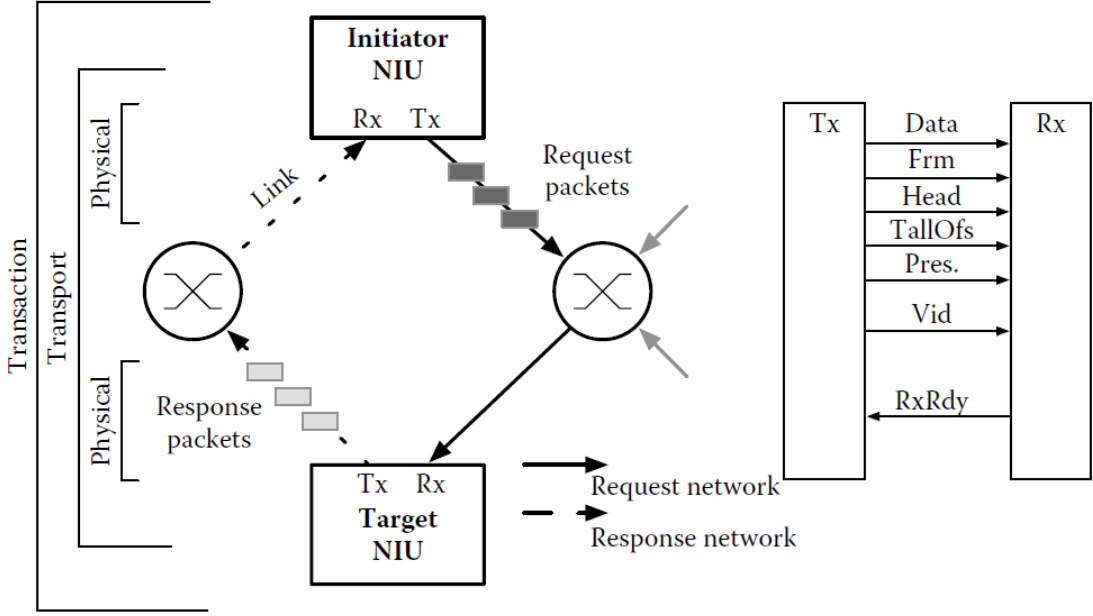
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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p>
configuring the first processing module having a first memory as a master the provides requests;	<p>The Arteris NoC utilized by the Snapdragon SoC configures the first processing module having a first memory as a master the provides requests, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris</p>

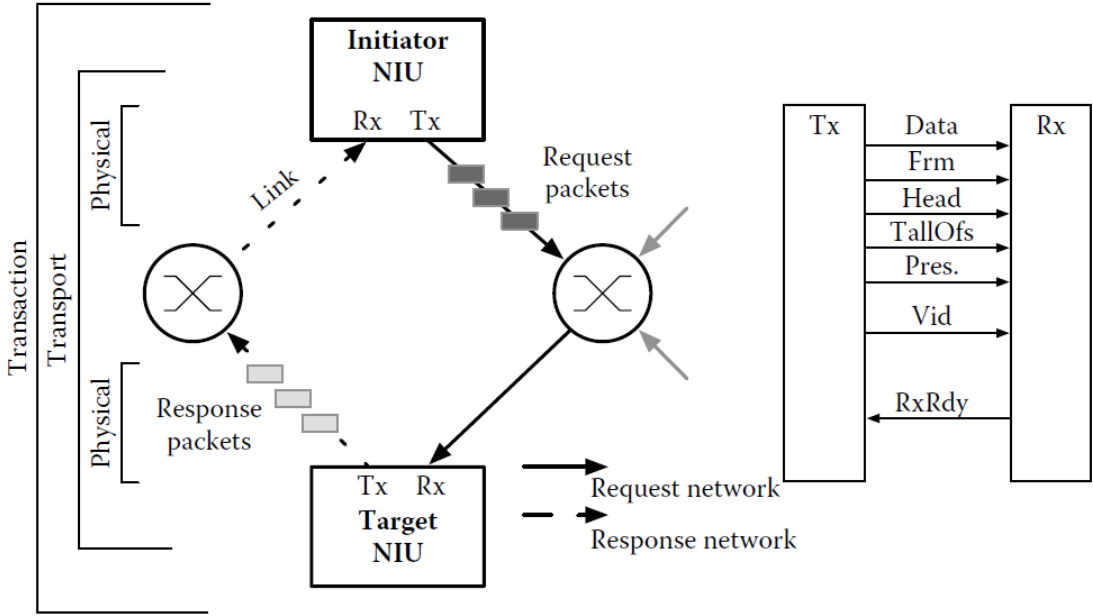
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	<p>NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p> <p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU’s Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Initiator NIUs are “used to connect a master node to the NoC”:</p>

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	<p data-bbox="520 261 1094 302">11.3.2 Network Interface Units</p> <p data-bbox="520 334 1856 472">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 513 1808 708" style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="499 735 1808 808">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="499 854 1887 1008">As a further example, “Initiator NIU units...enable connection between an AMBA-AHB master IP and the NoC [and] translate[] AHB transactions AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP” and has a “FIFO memory [...] inserted in the datapath for AHB write access”:</p>

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	<p>11.3.2.1 Initiator NIU Units</p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can</p>

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	<p>burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is</p> <ul style="list-style-type: none"> • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

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	<p style="text-align: center;">NIU Architecture</p> <p>The diagram illustrates the NIU Architecture, which is divided into two main sections: the Request Path and the Response Path. Both paths are connected to an AHB Slave Interface on the left. The Request Path starts with an 'AHB Req' arrow pointing into the interface. It then flows through a 'PIPE' block, which connects to a 'TRANSLATION TABLE'. The 'TRANSLATION TABLE' outputs 'Ctrl' to a 'BUILD HEADER & NECKER' block. Simultaneously, 'Data' from the 'AHB Req' flows into a 'DATA FIFO', which then connects to a 'Packet Assembly' block. The output of the 'Packet Assembly' goes to a 'PIPE bw/lw' block, which finally connects to the 'Tx Port' on the right. The Response Path starts from the 'Rx Port' on the right, which connects to a 'WIDTH CONVERTER' (shown in a dashed box). The output of the 'WIDTH CONVERTER' goes to a 'PIPE' block, which then connects to a 'FLOW CONTROL' block. The 'FLOW CONTROL' block outputs 'Information from request path' to the 'BUILD HEADER & NECKER' block. The 'FLOW CONTROL' block also outputs 'CONTROL' to the 'PIPE bw/lw' block. Finally, the 'FLOW CONTROL' block outputs an 'AHB Resp' arrow back to the AHB Slave Interface.</p> <p>FIGURE 11.4 Network interface unit: Initiator architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317-318.</p>
configuring the second processing module having a second memory as	The Arteris NoC utilized by the Snapdragon SoC configures the second processing module having a second memory as a slave the provides responses to the requests, either literally or under the doctrine of equivalents.

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“Integrated circuit and method for buffering to optimize burst length in networks on chips”

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
a slave the provides responses to the requests;	<p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

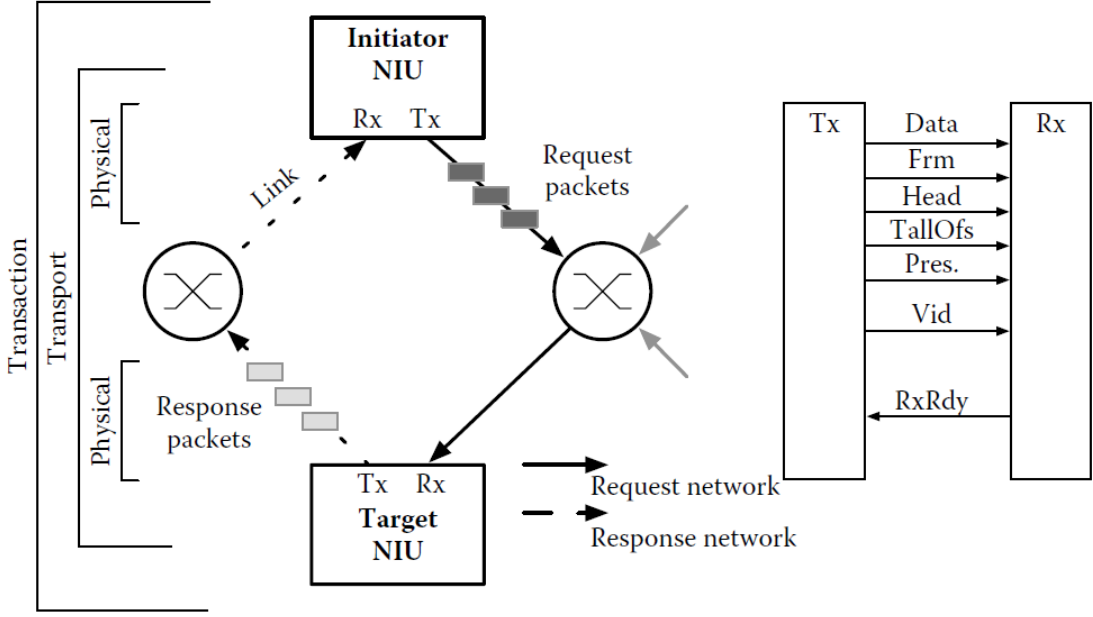
U.S. Patent No. 8,086,800 (Radulescu and Goossens)

“Integrated circuit and method for buffering to optimize burst length in networks on chips”

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Target NIUs are “used to connect a slave node to the NoC”:</p>

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	<p data-bbox="520 261 1094 302">11.3.2 Network Interface Units</p> <p data-bbox="520 334 1856 472">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 513 1808 708" style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="499 735 1808 808">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="499 854 1850 967">As further example, “Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets” and have a FIFO memory in the datapath:</p>

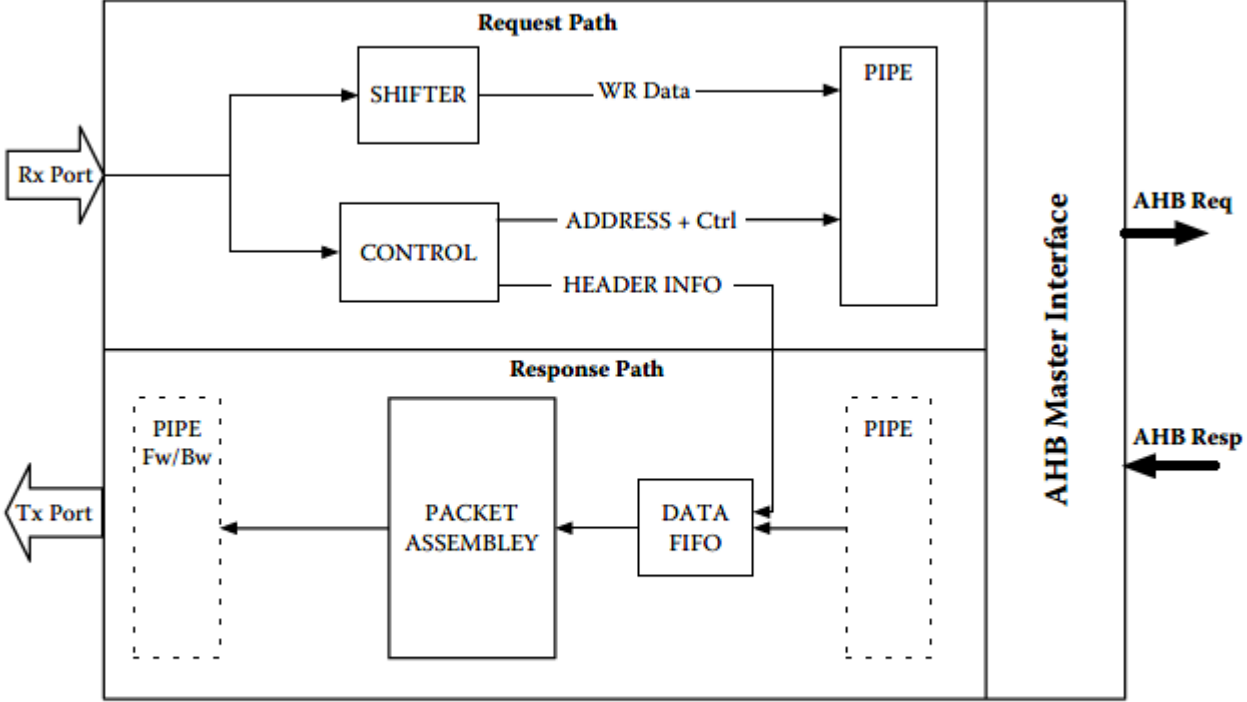
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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>11.3.2.2 Target NIU Units</p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always 32 bits wide, but the actual address space size may be downsized by setting a hardware parameter. Unused AHB address bits are then driven to zero. The NTTP request packet is then translated into one or more corresponding AHB accesses, depending on the transaction type (word aligned or nonaligned access). For example, if the request is an atomic Store, or a Load that can fit an AHB burst of specified length, then such a burst is generated. Otherwise, an AHB burst with unspecified length is generated.</p>

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	<p style="text-align: center;">Target NIU Architecture</p>  <p>The diagram illustrates the Target NIU Architecture. It is divided into two main horizontal sections: the Request Path (top) and the Response Path (bottom). On the left, there is an Rx Port (input) and a Tx Port (output). The Request Path contains a SHIFTER and a CONTROL block. The SHIFTER outputs WR Data to a PIPE. The CONTROL block outputs ADDRESS + Ctrl and HEADER INFO to the same PIPE. The Response Path contains a DATA FIFO, a PACKET ASSEMBLY, and two dashed boxes labeled PIPE Fw/Bw. The DATA FIFO outputs to the PACKET ASSEMBLY, which then outputs to the left PIPE Fw/Bw. The PACKET ASSEMBLY also outputs to the right PIPE Fw/Bw. The HEADER INFO from the Request Path is fed into the DATA FIFO. On the right, the AHB Master Interface connects to the system, with AHB Req (request) and AHB Resp (response) signals.</p> <p>FIGURE 11.5 Network interface unit: Target architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 318-319.</p>
connecting the master to a master	The Arteris NoC utilized by the Snapdragon SoC connects the master to a master interface unit of the interface units, either literally or under the doctrine of equivalents.

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interface unit of the interface units;	<p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

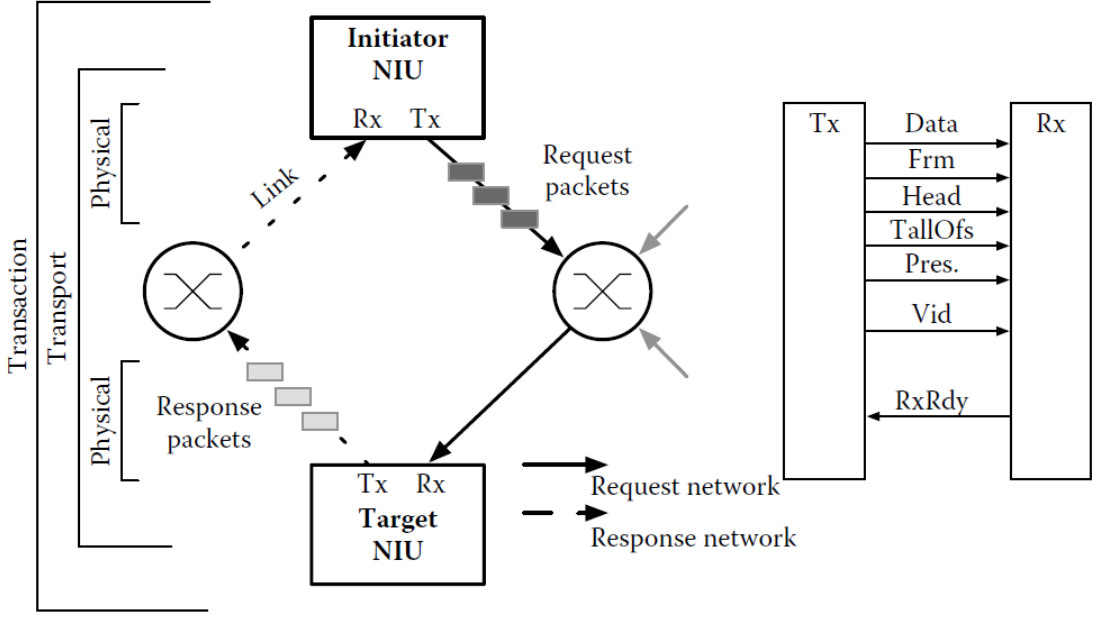
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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Initiator NIUs are “used to connect a master node to the NoC”:</p>

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	<p data-bbox="520 261 1094 302">11.3.2 Network Interface Units</p> <p data-bbox="520 334 1856 472">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 513 1808 708" style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="499 735 1808 808">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="499 854 1879 927">As a further example, “Initiator NIU units...enable connection between an AMBA-AHB master IP and the NoC”:</p>

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	<p>11.3.2.1 Initiator NIU Units</p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can</p>

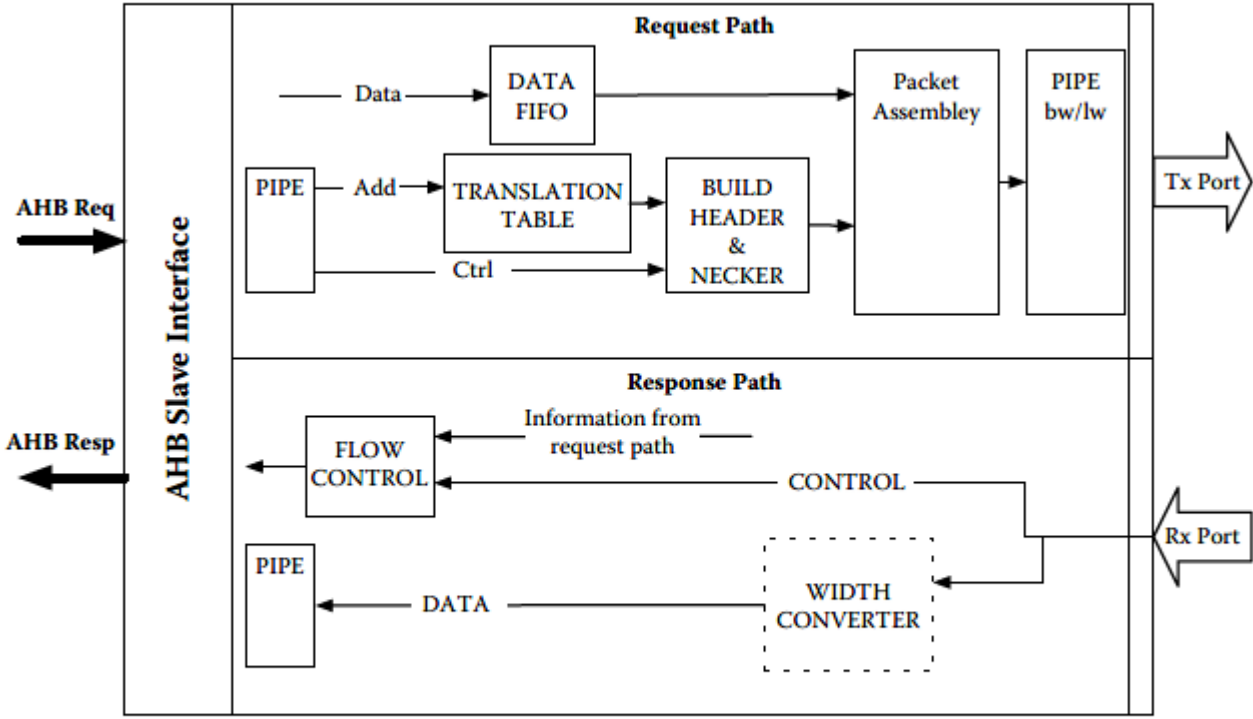
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	<p>burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is</p> <ul style="list-style-type: none"> • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

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	<p style="text-align: center;">NIU Architecture</p>  <p>FIGURE 11.4 Network interface unit: Initiator architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317-318.</p>
connecting the master interface unit to the	The Arteris NoC utilized by the Snapdragon SoC connects the master interface unit to the interconnect so that the master interface unit is between the master and the interconnect, either literally or under the doctrine of equivalents.

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
interconnect so that the master interface unit is between the master and the interconnect;	<p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

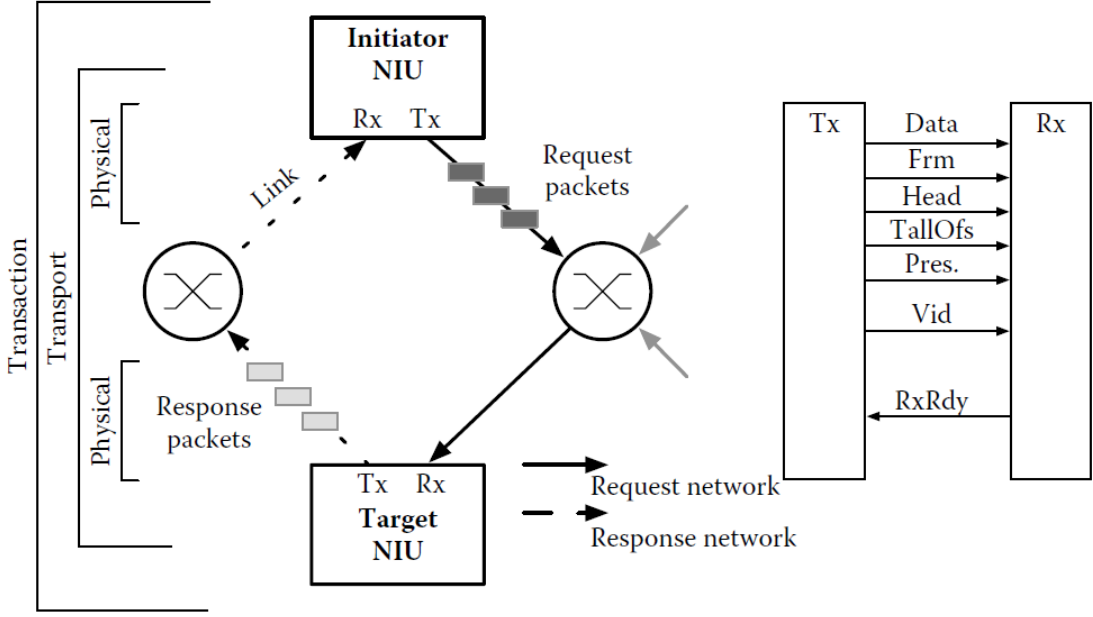
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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Initiator NIUs are “used to connect a master node to the NoC”:</p>

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	<p data-bbox="520 261 1094 302">11.3.2 Network Interface Units</p> <p data-bbox="520 334 1856 472">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 513 1808 708" style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="499 735 1808 808">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="499 894 1877 967">As a further example, “Initiator NIU units...enable connection between an AMBA-AHB master IP and the NoC”:</p>

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	<p>11.3.2.1 Initiator NIU Units</p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can</p>

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	<p style="text-align: center;">NIU Architecture</p> <p>FIGURE 11.4 Network interface unit: Initiator architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317-318.</p>
connecting the slave to a slave	The Arteris NoC utilized by the Snapdragon SoC connecting the slave to a slave interface unit of the interface units, either literally or under the doctrine of equivalents.

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interface unit of the interface units;	<p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

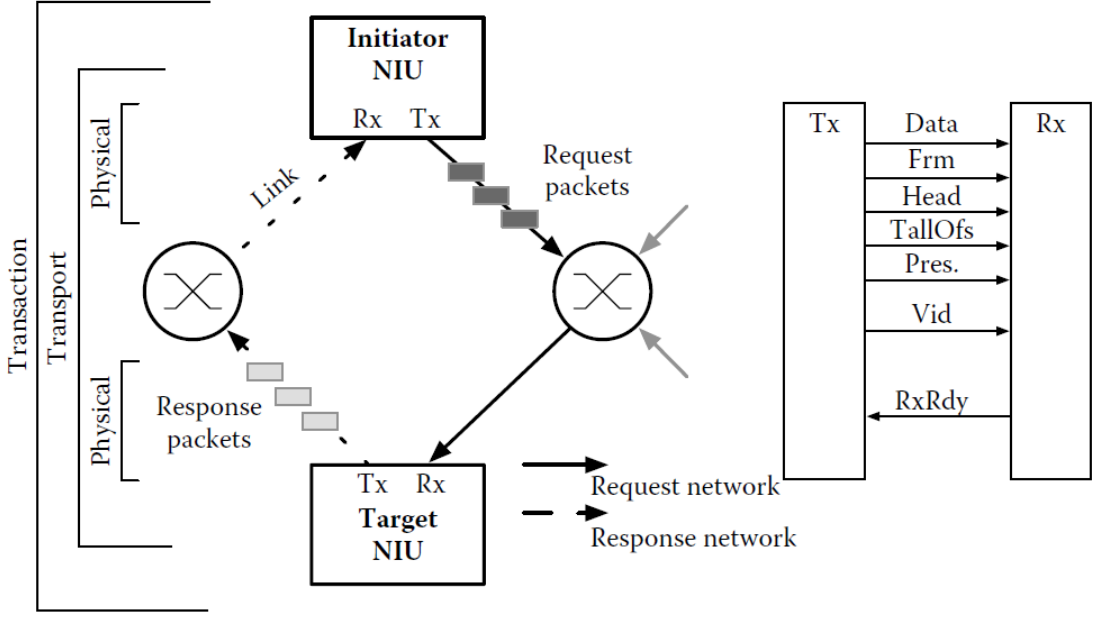
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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	<p data-bbox="520 261 1094 302">11.3.2 Network Interface Units</p> <p data-bbox="520 334 1856 472">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 513 1808 708" style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="499 735 1808 808">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="499 894 1850 1008">As further example, “Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets”:</p>

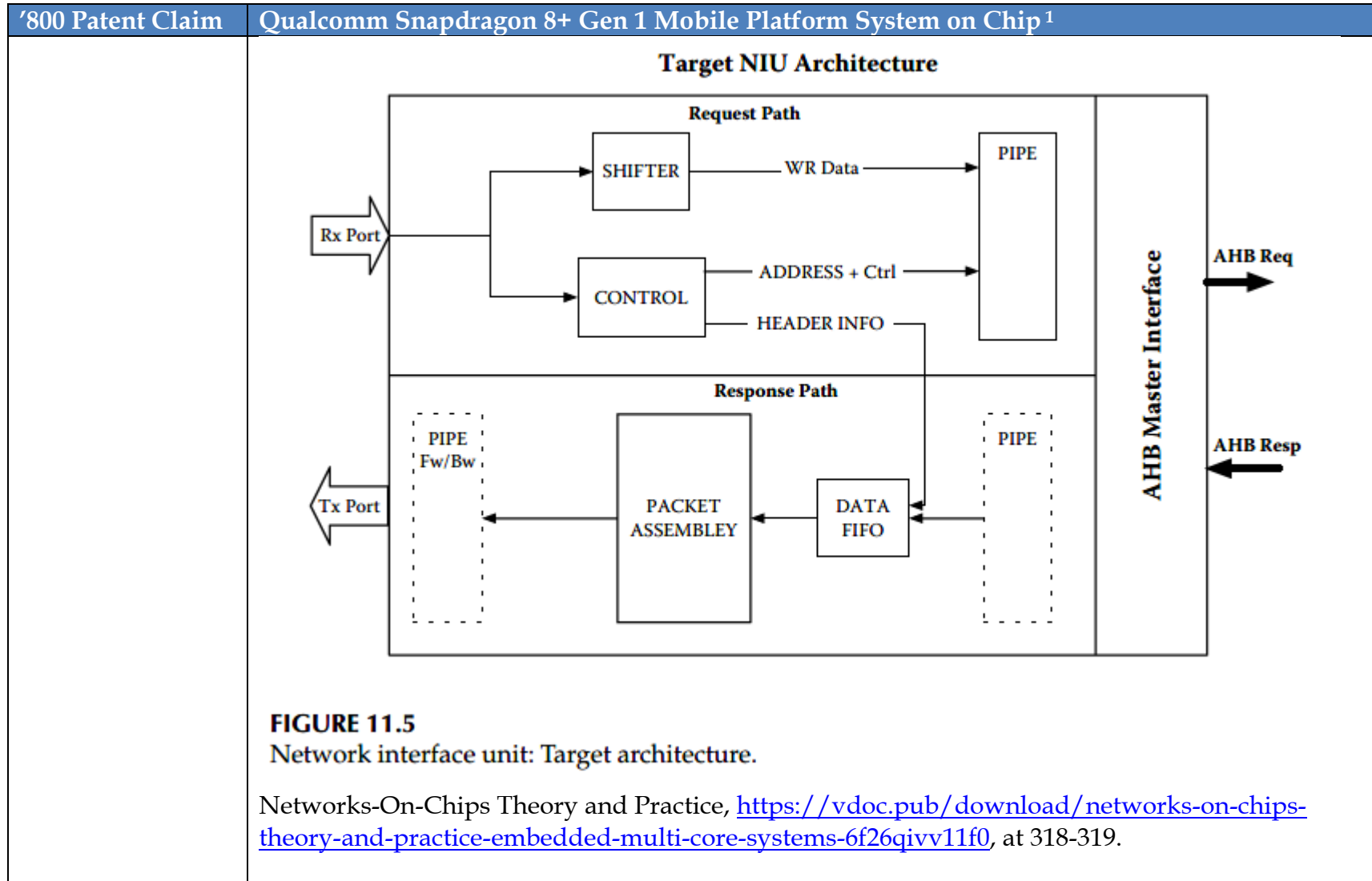
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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
connecting the slave interface unit to the interconnect so that the slave interface unit is between the slave and the interconnect;	<p>The Arteris NoC utilized by the Snapdragon SoC connects the slave interface unit to the interconnect so that the slave interface unit is between the slave and the interconnect, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

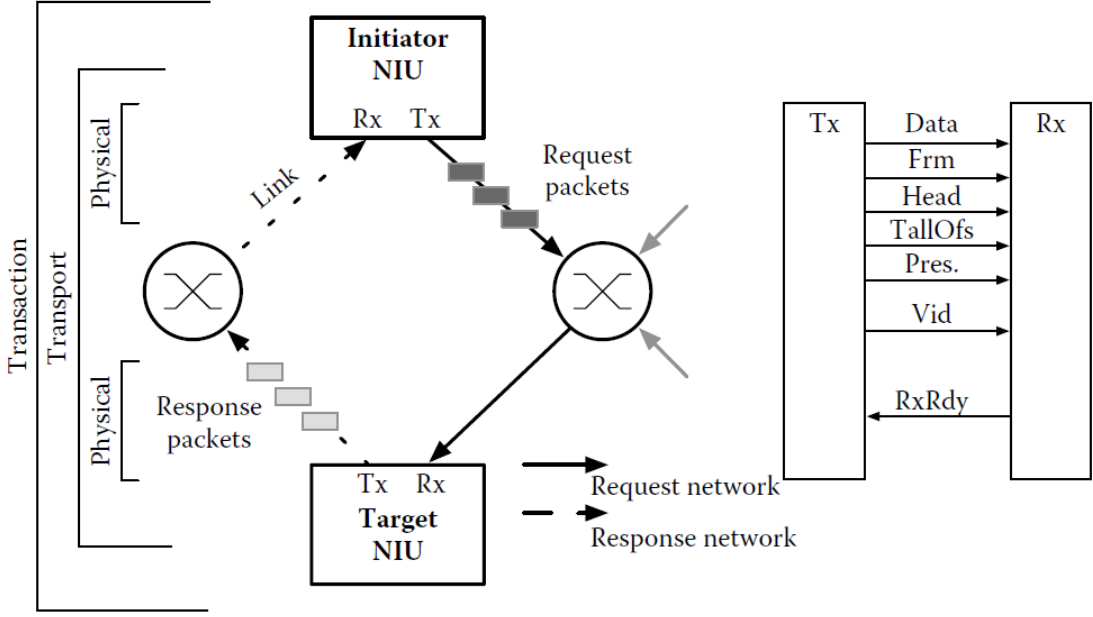
U.S. Patent No. 8,086,800 (Radulescu and Goossens)

“Integrated circuit and method for buffering to optimize burst length in networks on chips”

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Target NIUs are “used to connect a slave node to the NoC”:</p>

U.S. Patent No. 8,086,800 (Radulescu and Goossens)

“Integrated circuit and method for buffering to optimize burst length in networks on chips”

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p data-bbox="520 261 1094 302">11.3.2 Network Interface Units</p> <p data-bbox="520 334 1856 472">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 513 1808 708" style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="499 735 1808 808">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="499 854 1850 967">As further example, “Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets”:</p>

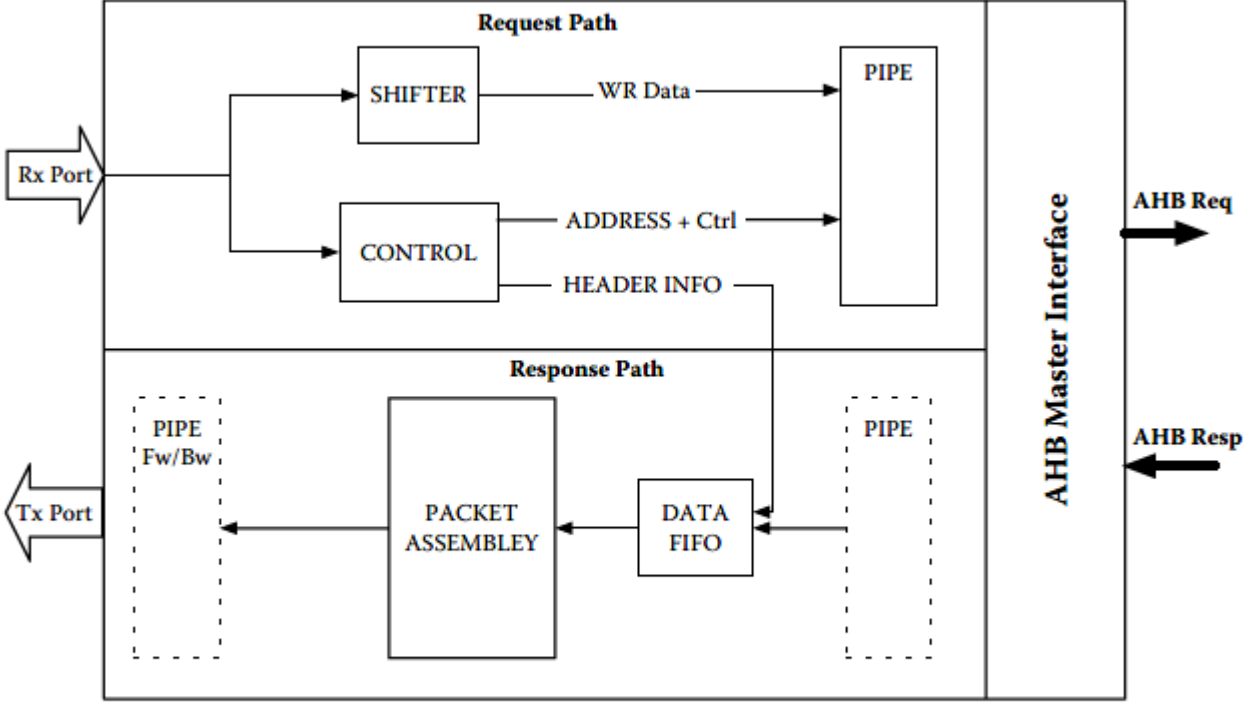
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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>11.3.2.2 Target NIU Units</p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always 32 bits wide, but the actual address space size may be downsized by setting a hardware parameter. Unused AHB address bits are then driven to zero. The NTTP request packet is then translated into one or more corresponding AHB accesses, depending on the transaction type (word aligned or nonaligned access). For example, if the request is an atomic Store, or a Load that can fit an AHB burst of specified length, then such a burst is generated. Otherwise, an AHB burst with unspecified length is generated.</p>

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p style="text-align: center;">Target NIU Architecture</p>  <p>The diagram illustrates the Target NIU Architecture. It is divided into two main horizontal sections: the Request Path (top) and the Response Path (bottom). On the left, there is an Rx Port (input) and a Tx Port (output). The Request Path contains a SHIFTER and a CONTROL block. The Rx Port feeds into both. The SHIFTER outputs WR Data to a PIPE. The CONTROL block outputs ADDRESS + Ctrl to the same PIPE and HEADER INFO to a DATA FIFO in the Response Path. The Response Path contains a PACKET ASSEMBLY, a DATA FIFO, and two dashed boxes labeled PIPE Fw/Bw. The DATA FIFO receives data from the PIPE in the Request Path and outputs to the PACKET ASSEMBLY. The PACKET ASSEMBLY outputs to the Tx Port. The Tx Port also feeds into the left PIPE Fw/Bw block. On the right, the AHB Master Interface connects to the system bus, with AHB Req (request) and AHB Resp (response) signals.</p> <p>FIGURE 11.5 Network interface unit: Target architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 318-319.</p>

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
<p>determining by a master determination unit of the master interface unit a first optimal amount of data to be buffered by a master wrapper of the master interface unit;</p>	<p>The Arteris NoC utilized by the Snapdragon SoC determines by a master determination unit of the master interface unit a first optimal amount of data to be buffered by a master wrapper of the master interface unit, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

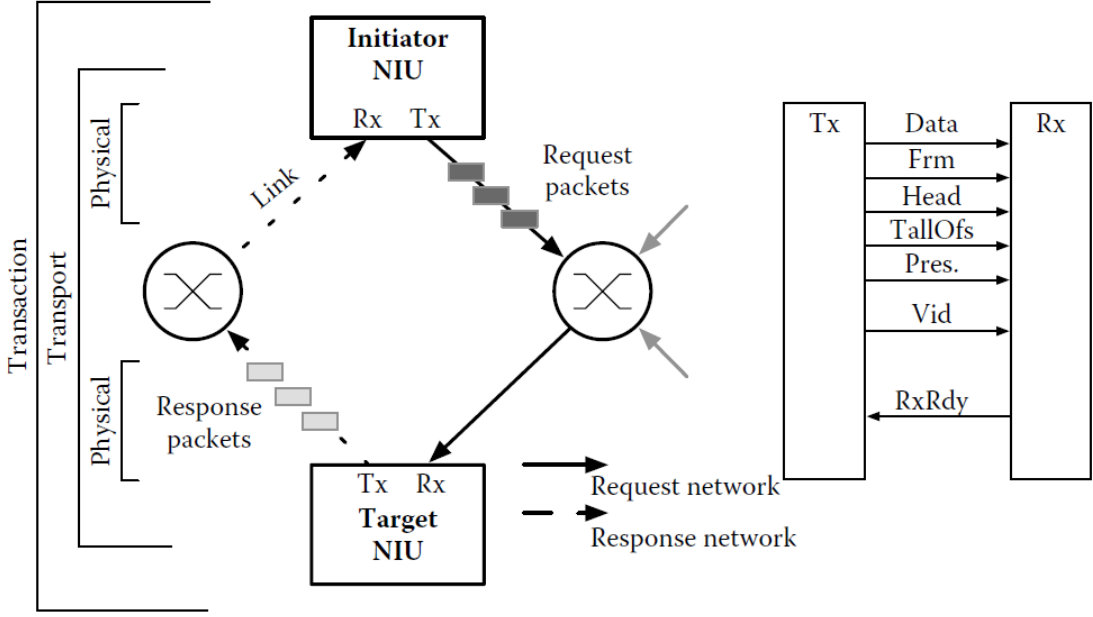
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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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“Integrated circuit and method for buffering to optimize burst length in networks on chips”

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Initiator NIUs are “used to connect a master node to the NoC”:</p>

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p data-bbox="520 261 1094 302">11.3.2 Network Interface Units</p> <p data-bbox="520 334 1856 472">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 513 1808 708" style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="499 735 1808 808">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="499 854 1835 967">In the Arteris NoC “Initiator NIU units...enable connection between an AMBA-AHB master IP and the NoC” and includes blocks such as “Data FIFO,” “Translation Table,” “Build Header & Necker,” and “Packet Assembly”:</p>

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p style="text-align: center;">NIU Architecture</p> <p>FIGURE 11.4 Network interface unit: Initiator architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.</p> <p>In the Initiator NIUs of the Arteris NoC, a “FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can burst at NoC rate as soon as a minimum amount of data has been received.” “[T]he FIFO depth is</p>

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p data-bbox="506 253 1860 326">defined by the hardware parameter” which “indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port”:</p> <p data-bbox="531 391 1024 427">11.3.2.1 Initiator NIU Units</p> <p data-bbox="527 451 1812 1084">Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p data-bbox="527 1089 1812 1174">A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can</p>

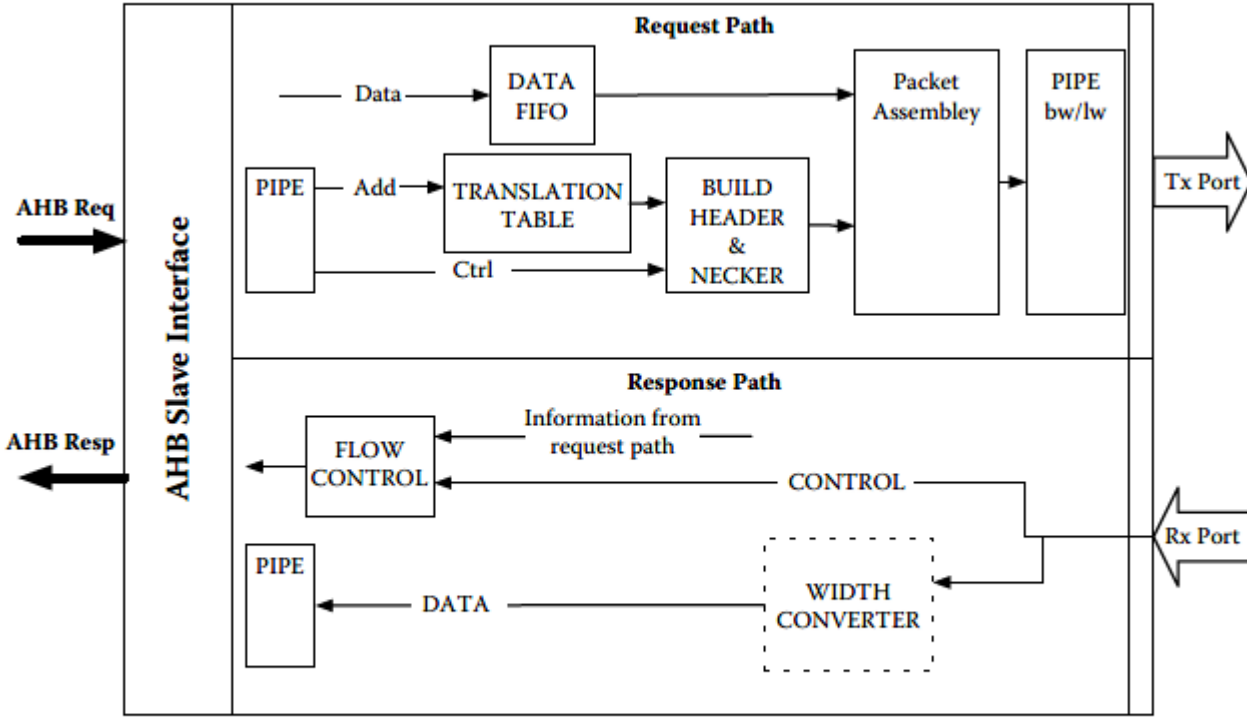
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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is</p> <ul style="list-style-type: none"> • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

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"Integrated circuit and method for buffering to optimize burst length in networks on chips"

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p style="text-align: center;">NIU Architecture</p>  <p>FIGURE 11.4 Network interface unit: Initiator architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317-318.</p>
determining by a slave determination unit	The Arteris NoC utilized by the Snapdragon SoC determines by a slave determination unit of the slave interface unit a second optimal amount of data to be buffered by a slave wrapper of the slave interface unit, either literally or under the doctrine of equivalents.

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
<p>of the slave interface unit a second optimal amount of data to be buffered by a slave wrapper of the slave interface unit;</p>	<p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

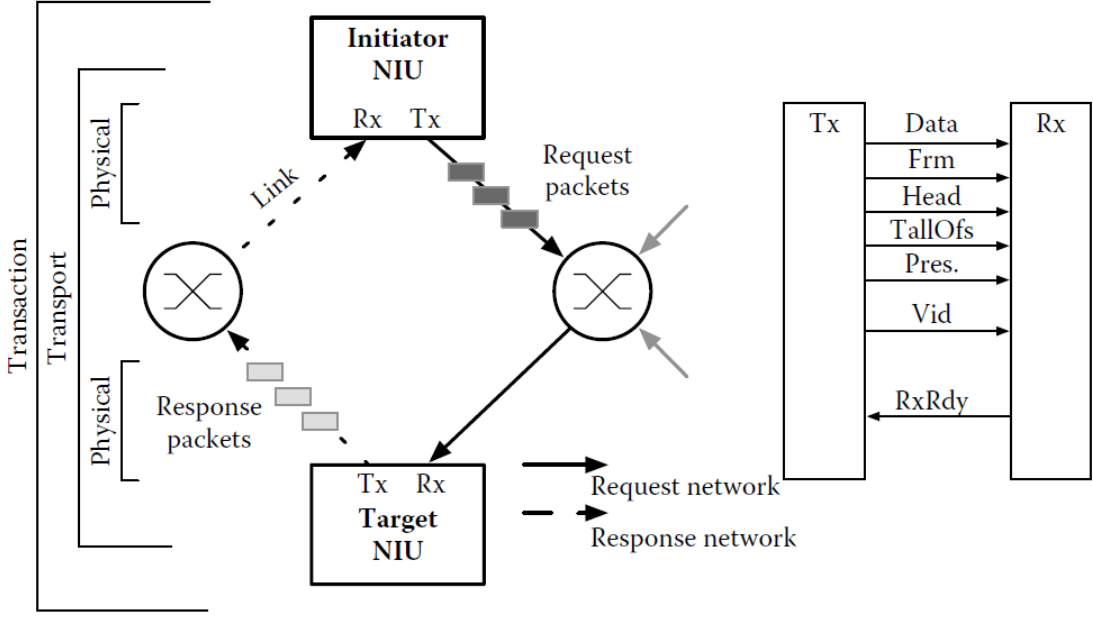
U.S. Patent No. 8,086,800 (Radulescu and Goossens)

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Target NIUs are “used to connect a slave node to the NoC”:</p>

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p data-bbox="520 261 1094 302">11.3.2 Network Interface Units</p> <p data-bbox="520 334 1856 472">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 513 1808 708" style="list-style-type: none"> <li data-bbox="594 513 1808 594">• Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC <li data-bbox="594 618 1808 708">• Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="499 735 1808 808">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="499 854 1871 967">As further example, “Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets” and includes blocks such as “Data FIFO ”and “Packet Assembly”:</p>

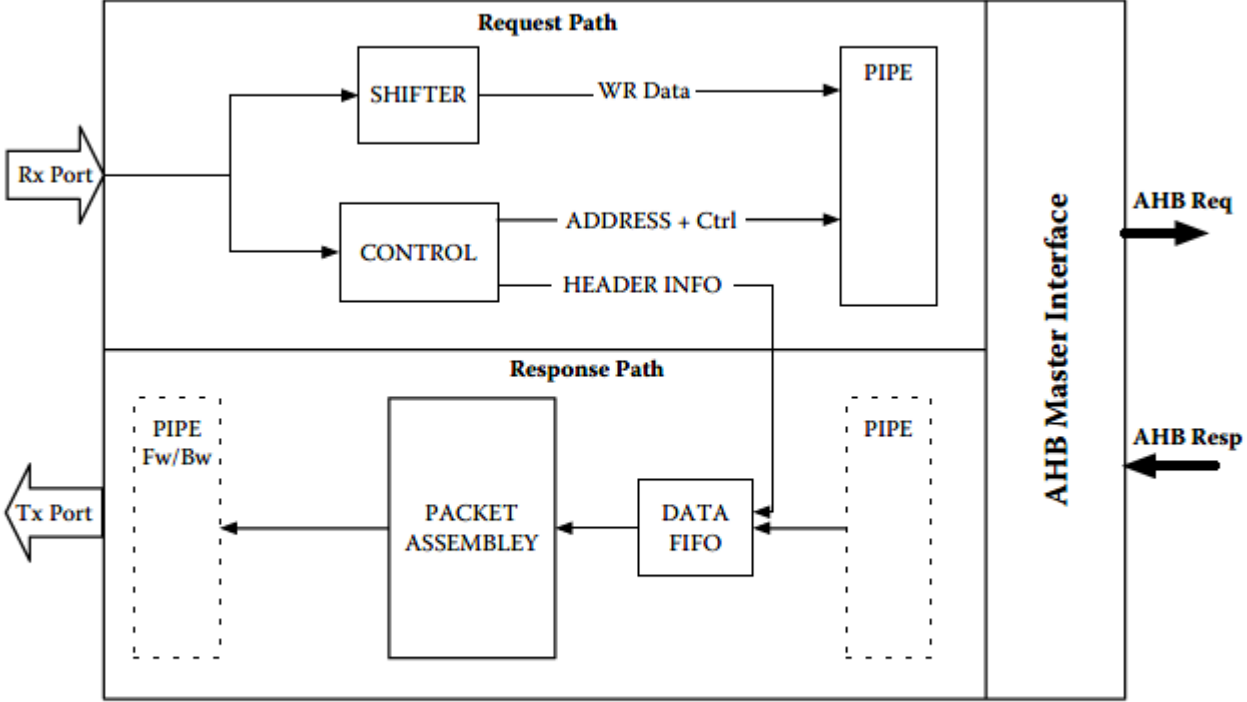
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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>11.3.2.2 Target NIU Units</p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always 32 bits wide, but the actual address space size may be downsized by setting a hardware parameter. Unused AHB address bits are then driven to zero. The NTTP request packet is then translated into one or more corresponding AHB accesses, depending on the transaction type (word aligned or nonaligned access). For example, if the request is an atomic Store, or a Load that can fit an AHB burst of specified length, then such a burst is generated. Otherwise, an AHB burst with unspecified length is generated.</p>

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	<p style="text-align: center;">Target NIU Architecture</p>  <p>The diagram illustrates the Target NIU Architecture. It is divided into two main horizontal sections: the Request Path (top) and the Response Path (bottom). On the left, there is an Rx Port (input) and a Tx Port (output). The Request Path contains a SHIFTER and a CONTROL block. The Rx Port feeds into both. The SHIFTER outputs WR Data to a PIPE. The CONTROL block outputs ADDRESS + Ctrl to the same PIPE and HEADER INFO to a DATA FIFO in the Response Path. The Response Path contains a PACKET ASSEMBLY and two dashed boxes labeled PIPE Fw/Bw. The DATA FIFO feeds into the PACKET ASSEMBLY, which then feeds into the left PIPE Fw/Bw. The PACKET ASSEMBLY also feeds into the Tx Port. On the right, the AHB Master Interface connects to the system bus, with AHB Req (request) and AHB Resp (response) signals.</p> <p>FIGURE 11.5 Network interface unit: Target architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 318-319.</p>

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“Integrated circuit and method for buffering to optimize burst length in networks on chips”

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>In the Target NIUs of the Arteris NoC, similar to as described above for the Initiator NIUs, “[a] FIFO memory is inserted in the datapath for AHB ... accesses. The FIFO memory absorbs data at the AHB ... rate, so that NTTP packets can burst at NoC rate as soon as a minimum amount of data has been received.” “[T]he FIFO depth is defined by the hardware parameter” which “indicates the amount of data required to generate a ... packet: each time the FIFO is full, a ... packet is sent on the Tx port”:</p> <p>A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is</p> <ul style="list-style-type: none"> • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

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	Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0 , at 317-318.
buffering by the slave wrapper of the slave interface unit data from the slave to be transferred over the interconnect until a first optimal amount of data is buffered;	<p>The Arteris NoC utilized by the Snapdragon SoC buffers by the slave wrapper of the slave interface unit data from the slave to be transferred over the interconnect until a first optimal amount of data is buffered, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

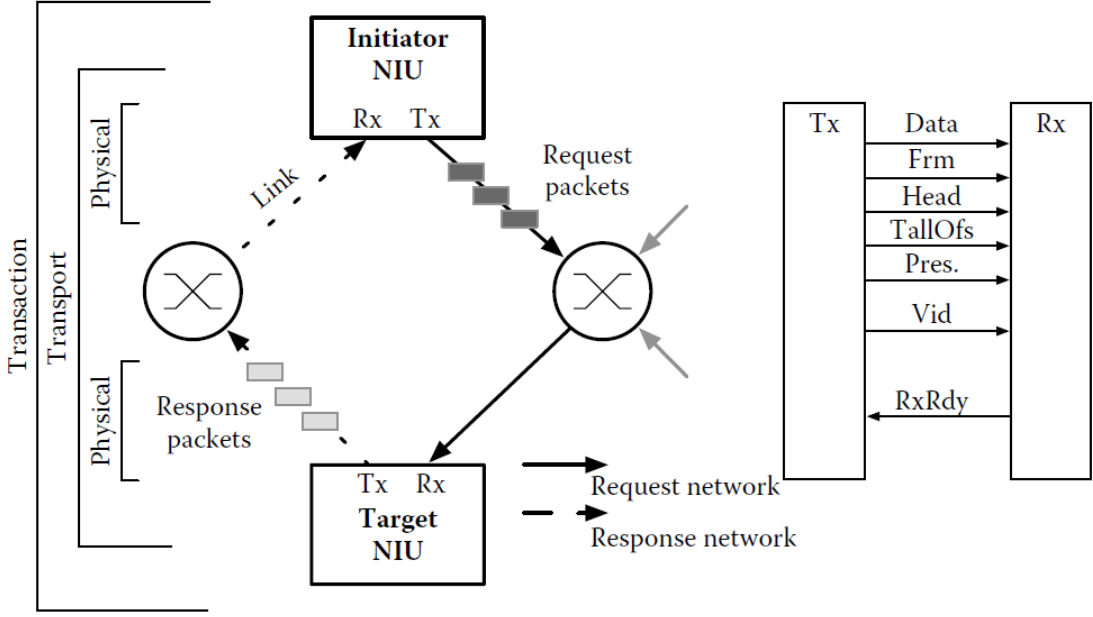
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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Target NIUs are “used to connect a slave node to the NoC”:</p>

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	<p data-bbox="520 261 1094 302">11.3.2 Network Interface Units</p> <p data-bbox="520 334 1856 472">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 513 1808 708" style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="499 735 1808 808">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="499 854 1871 967">As further example, “Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets” and includes blocks such as “Data FIFO ”and “Packet Assembly”:</p>

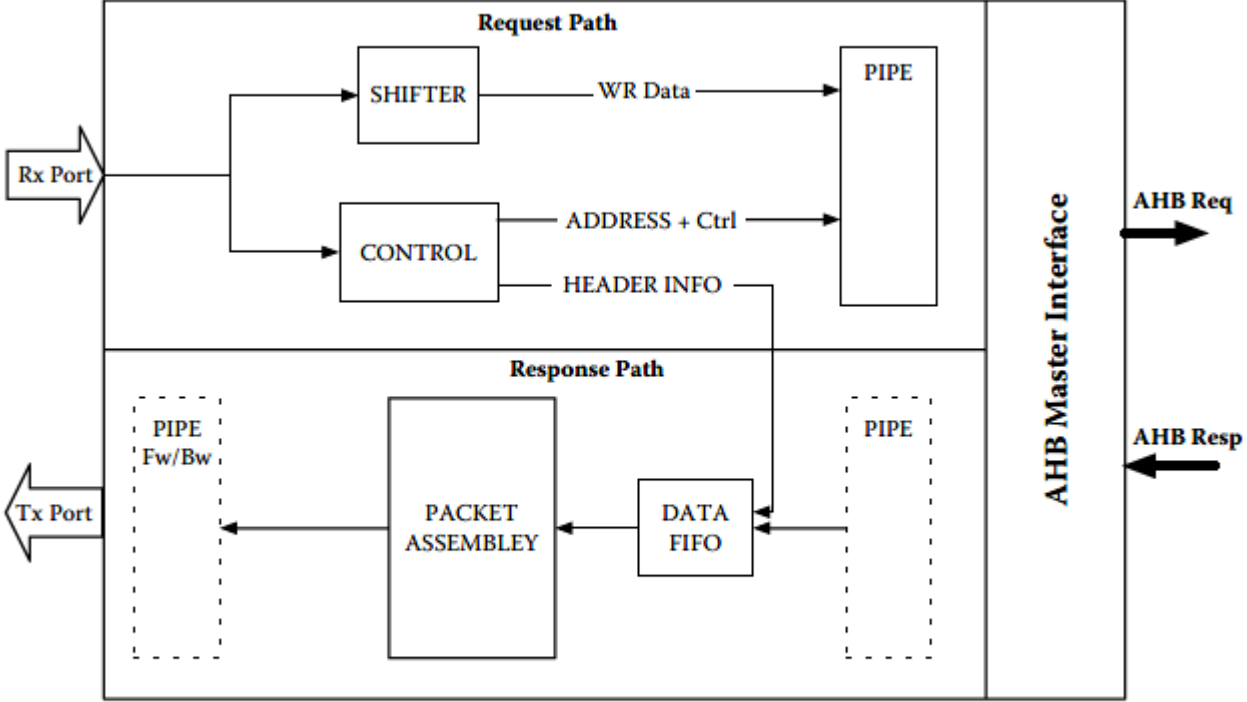
U.S. Patent No. 8,086,800 (Radulescu and Goossens)

“Integrated circuit and method for buffering to optimize burst length in networks on chips”

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>11.3.2.2 Target NIU Units</p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always 32 bits wide, but the actual address space size may be downsized by setting a hardware parameter. Unused AHB address bits are then driven to zero. The NTTP request packet is then translated into one or more corresponding AHB accesses, depending on the transaction type (word aligned or nonaligned access). For example, if the request is an atomic Store, or a Load that can fit an AHB burst of specified length, then such a burst is generated. Otherwise, an AHB burst with unspecified length is generated.</p>

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	<p style="text-align: center;">Target NIU Architecture</p>  <p>The diagram illustrates the Target NIU Architecture. It is divided into two main horizontal sections: the Request Path (top) and the Response Path (bottom). On the left, there is an Rx Port (input) and a Tx Port (output). The Request Path contains a SHIFTER and a CONTROL block. The Rx Port feeds into both. The SHIFTER outputs WR Data to a PIPE. The CONTROL block outputs ADDRESS + Ctrl to the same PIPE and HEADER INFO to a DATA FIFO. The Response Path contains a PACKET ASSEMBLY and a DATA FIFO. The DATA FIFO receives data from the PIPE and outputs to the PACKET ASSEMBLY. The PACKET ASSEMBLY outputs to a dashed box labeled PIPE Fw/Bw, which then feeds into the Tx Port. On the right, the AHB Master Interface connects to the system bus, with AHB Req (request) and AHB Resp (response) signals.</p> <p>FIGURE 11.5 Network interface unit: Target architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 318-319.</p>

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	<p>In the Target NIUs of the Arteris NoC, similar to as described above for the Initiator NIUs, “[a] FIFO memory is inserted in the datapath for AHB ... accesses. The FIFO memory absorbs data at the AHB ... rate, so that NTTP packets can burst at NoC rate as soon as a minimum amount of data has been received.” “[T]he FIFO depth is defined by the hardware parameter” which “indicates the amount of data required to generate a ... packet: each time the FIFO is full, a ... packet is sent on the Tx port”:</p> <p>A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is</p> <ul style="list-style-type: none"> • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

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	<p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317-318.</p> <p>As a further illustration, the Arteris NoC uses “a mechanism called rated adaptation, which stalls packets just enough to remove wait states from the packets, preserving a low latency.” For other traffic, the “[b]est effort traffic can be left untouched[,]” “[l]atency sensitive traffic may have its urgency modulated as a function of the transaction[,]” “[s]oft real-time traffic may have its hurry level modulated as a function of the bandwidth it receives[,]” and “[o]n the real-time modem data port, the hurry is fixed at a critical level”:</p> <p>Those effects can be mended by the insertion of buffering. In the case of peak bandwidth reduction, a simple FIFO does the job: Busy states present at the output of the FIFO do not propagate back to the input until the FIFO is full. For a peak bandwidth increase, the situation is a bit more complex. In a FIFO, wait states present at the input are only absorbed when the FIFO is not empty. Arteris proposes a mechanism called rate adaptation, which stalls packets just enough to remove wait states from the packets, preserving a low latency.</p> <p>In this second step, the architecture is modified to introduce some buffering. In our example 760 bytes of memory have been distributed across the topology. Some have been put on existing links; some required the creation of new links.</p> <p>See Application driven network-on-chip architecture exploration & refinement for a complex SoC, https://www.arteris.com/hs-fs/hub/48858/file-14363521-pdf/docs/springerappdrivennocarchitecture8.5x11.pdf, at pg.16.</p>
transferring the buffered data from the slave wrapper to the master	<p>The Arteris NoC utilized by the Snapdragon SoC transfers the buffered data from the slave wrapper to the master wrapper when said first optimal amount of data has been buffered by the slave wrapper, either literally or under the doctrine of equivalents.</p>

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<p>wrapper when said first optimal amount of data has been buffered by the slave wrapper;</p>	<p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

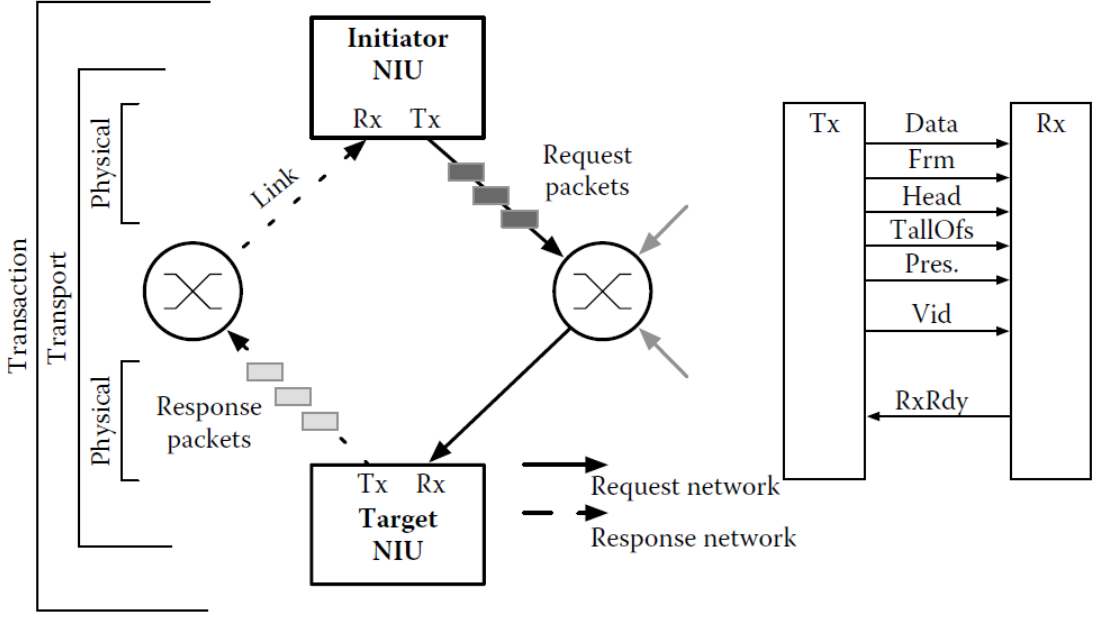
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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Target NIUs are “used to connect a slave node to the NoC”:</p>

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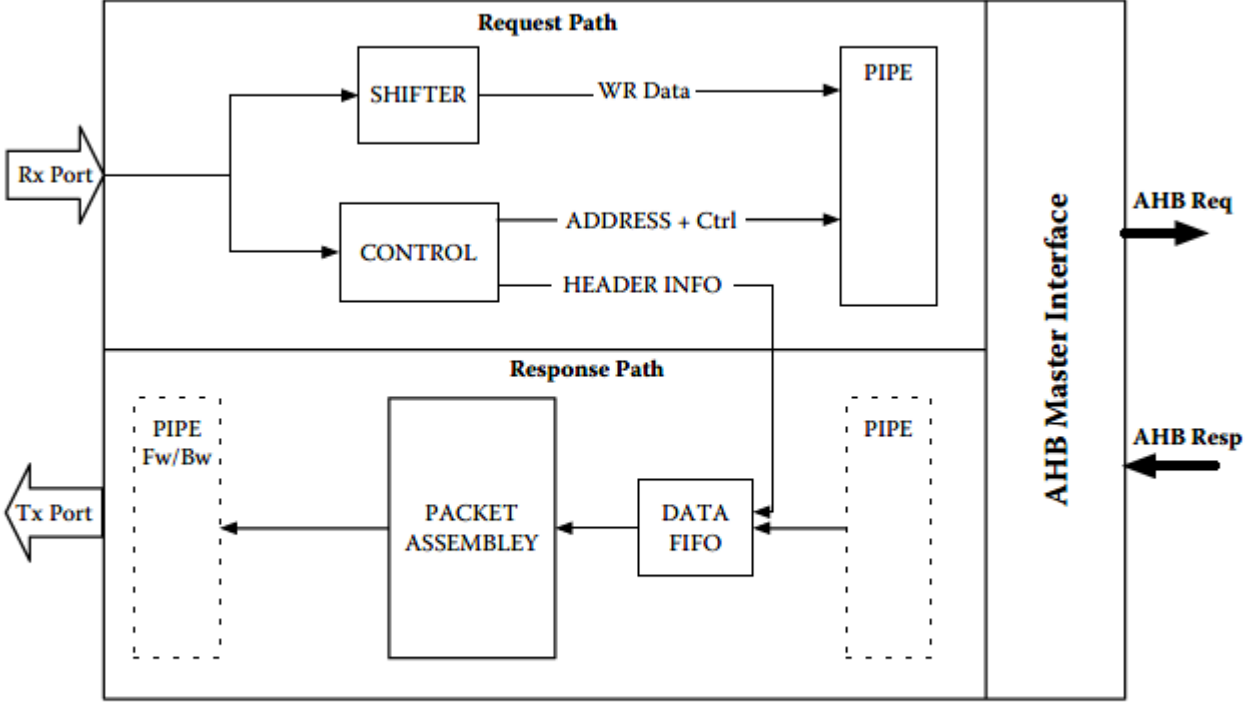
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buffering by the master wrapper of the master interface unit data from the master to be transferred over the interconnect until a second optimal amount of data is buffered by the master wrapper;	<p>The Arteris NoC utilized by the Snapdragon SoC buffers by the master wrapper of the master interface unit data from the master to be transferred over the interconnect until a second optimal amount of data is buffered by the master wrapper, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

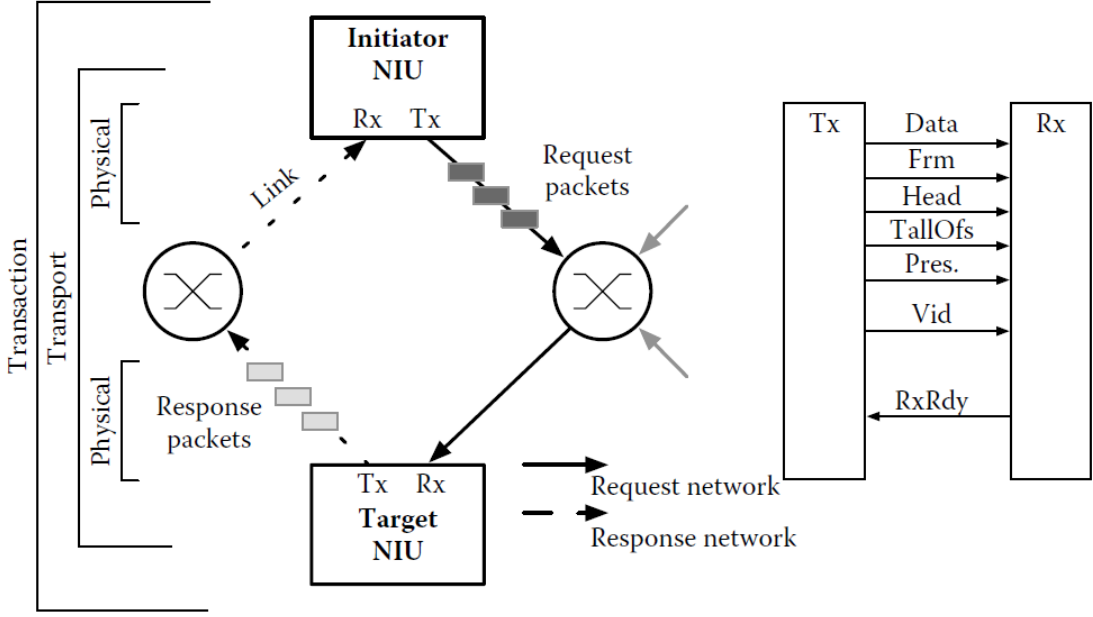
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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Initiator NIUs are “used to connect a master node to the NoC”:</p>

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	<p style="text-align: center;">NIU Architecture</p> <p>FIGURE 11.4 Network interface unit: Initiator architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.</p> <p>In the Initiator NIUs of the Arteris NoC, a “FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can burst at NoC rate as soon as a minimum amount of data has been received.” “[T]he FIFO depth is</p>

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	<p data-bbox="506 253 1860 326">defined by the hardware parameter” which “indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port”:</p> <p data-bbox="531 391 1024 427">11.3.2.1 Initiator NIU Units</p> <p data-bbox="527 448 1812 1081">Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p data-bbox="527 1089 1812 1174">A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can</p>

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transferring the buffered data from the master wrapper to the slave wrapper when said second optimal amount of data has been buffered by the master wrapper,	<p>The Arteris NoC utilized by the Snapdragon SoC transfers the buffered data from the master wrapper to the slave wrapper when said second optimal amount of data has been buffered by the master wrapper, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p>

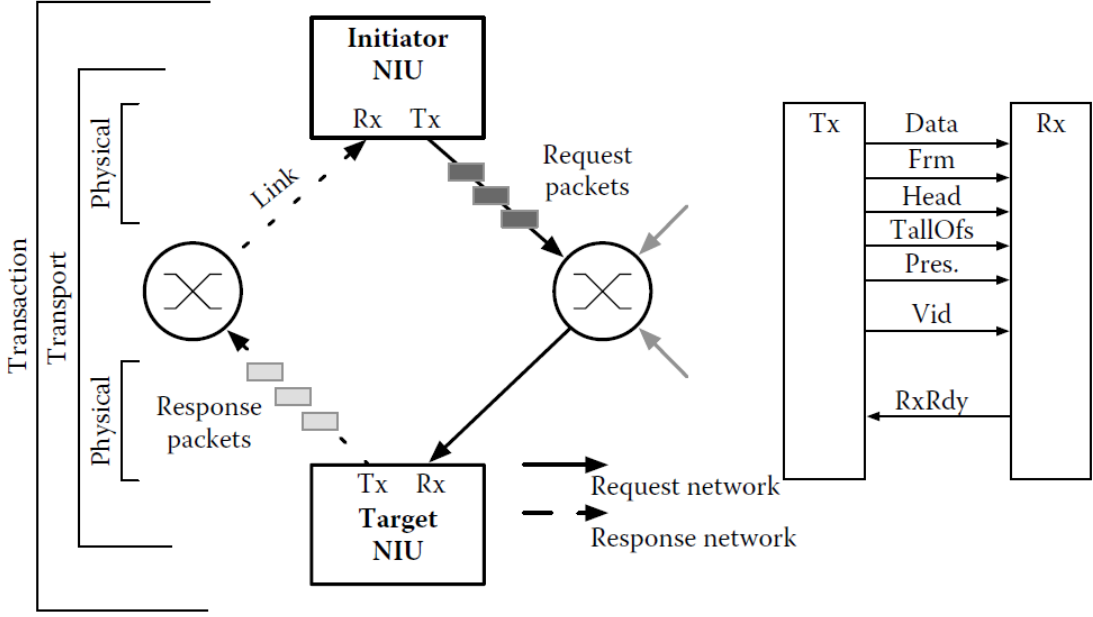
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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Initiator NIUs are “used to connect a master node to the NoC”:</p>

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'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p data-bbox="520 261 1094 302">11.3.2 Network Interface Units</p> <p data-bbox="520 334 1856 472">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 513 1808 708" style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="499 735 1808 808">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="499 854 1835 967">In the Arteris NoC “Initiator NIU units...enable connection between an AMBA-AHB master IP and the NoC” and includes blocks such as “Data FIFO,” “Translation Table,” “Build Header & Necker,” and “Packet Assembly”:</p>

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	<p style="text-align: center;">NIU Architecture</p> <p>FIGURE 11.4 Network interface unit: Initiator architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.</p> <p>In the Initiator NIUs of the Arteris NoC, a “FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can burst at NoC rate as soon as a minimum amount of data has been received.” “[T]he FIFO depth is</p>

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	<p>defined by the hardware parameter” which “indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port”:</p> <p>11.3.2.1 Initiator NIU Units</p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can</p>

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	<p>burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is</p> <ul style="list-style-type: none"> • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

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	<p style="text-align: center;">NIU Architecture</p> <p>FIGURE 11.4 Network interface unit: Initiator architecture. Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317-318.</p>
wherein at least one of the first determination unit	In the Arteris NoC utilized by the Snapdragon SoC, at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of

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<p>and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it</p>	<p>the communication between the master and the slave wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

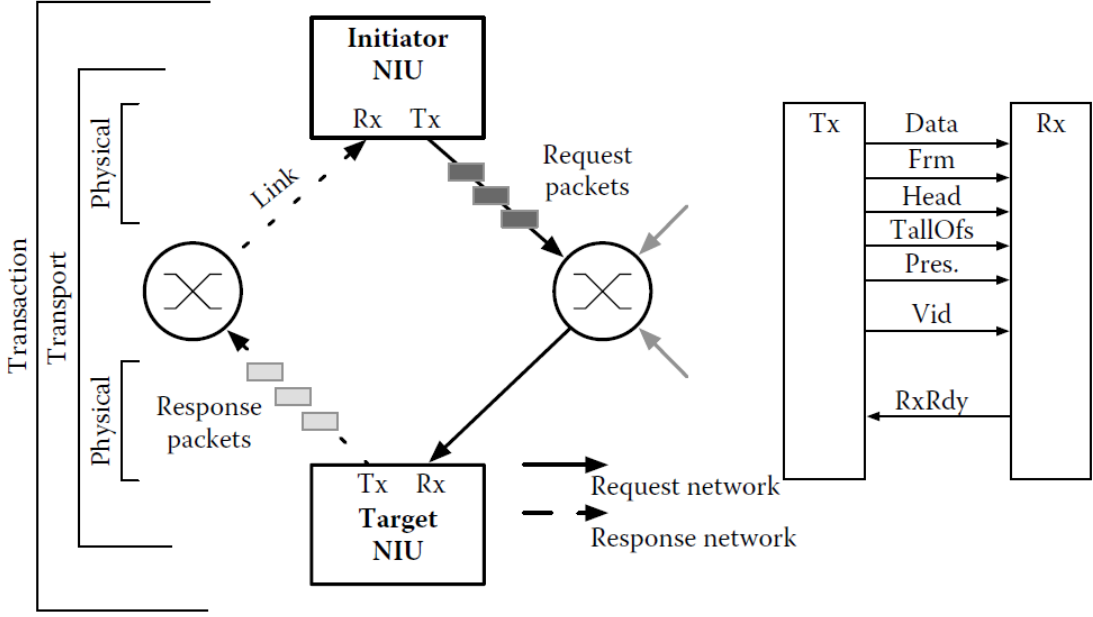
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<p>is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.</p>	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>The Initiator NIUs are “used to connect a master node to the NoC” and the Target NIUs are “used to connect a slave node to the NoC”:</p>

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	<p data-bbox="520 261 1094 302">11.3.2 Network Interface Units</p> <p data-bbox="520 334 1856 472">The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul data-bbox="594 513 1808 708" style="list-style-type: none"> • Initiator NIU—third party protocol-to-NTTP, used to connect a master node to the NoC • Target NIUs—NTTP-to-third party protocol, used to connect a slave node to the NoC <p data-bbox="499 735 1808 808">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317.</p> <p data-bbox="499 854 1835 967">In the Arteris NoC “Initiator NIU units...enable connection between an AMBA-AHB master IP and the NoC” and includes blocks such as “Data FIFO,” “Translation Table,” “Build Header & Necker,” and “Packet Assembly”:</p>

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	<p style="text-align: center;">NIU Architecture</p> <p>FIGURE 11.4 Network interface unit: Initiator architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.</p> <p>In the Initiator NIUs of the Arteris NoC, a "FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can burst at NoC rate as soon as a minimum amount of data has been received." "[T]he FIFO depth is</p>

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	<p data-bbox="499 250 1877 326">defined by the hardware parameter” which “indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port”:</p> <p data-bbox="531 386 1024 423">11.3.2.1 Initiator NIU Units</p> <p data-bbox="525 444 1812 1081">Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p data-bbox="525 1086 1812 1170">A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can</p>

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	<p>burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is</p> <ul style="list-style-type: none"> • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

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	<p style="text-align: center;">NIU Architecture</p> <p>The diagram illustrates the NIU Architecture, which is divided into two main sections: the Request Path and the Response Path. Both paths interface with an AHB Slave Interface on the left. The Request Path starts with an AHB Req signal entering the AHB Slave Interface. Data flows from the AHB Slave Interface into a DATA FIFO, then to a Packet Assembly block, and finally to a PIPE bw/lw block, which connects to the Tx Port. The Response Path starts with an AHB Resp signal entering the AHB Slave Interface. Data flows from the Rx Port into a WIDTH CONVERTER (dashed box), then to a PIPE block, and finally to a FLOW CONTROL block. The FLOW CONTROL block sends information back to the AHB Slave Interface. Additionally, there is a CONTROL signal path from the FLOW CONTROL block to the Packet Assembly block. A TRANSLATION TABLE and a BUILD HEADER & NECKER block are also shown, connected to the AHB Slave Interface and the Packet Assembly block.</p> <p>FIGURE 11.4 Network interface unit: Initiator architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317-318.</p> <p>As further example, “Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets” and includes blocks such as “Data FIFO ”and “Packet Assembly”:</p>

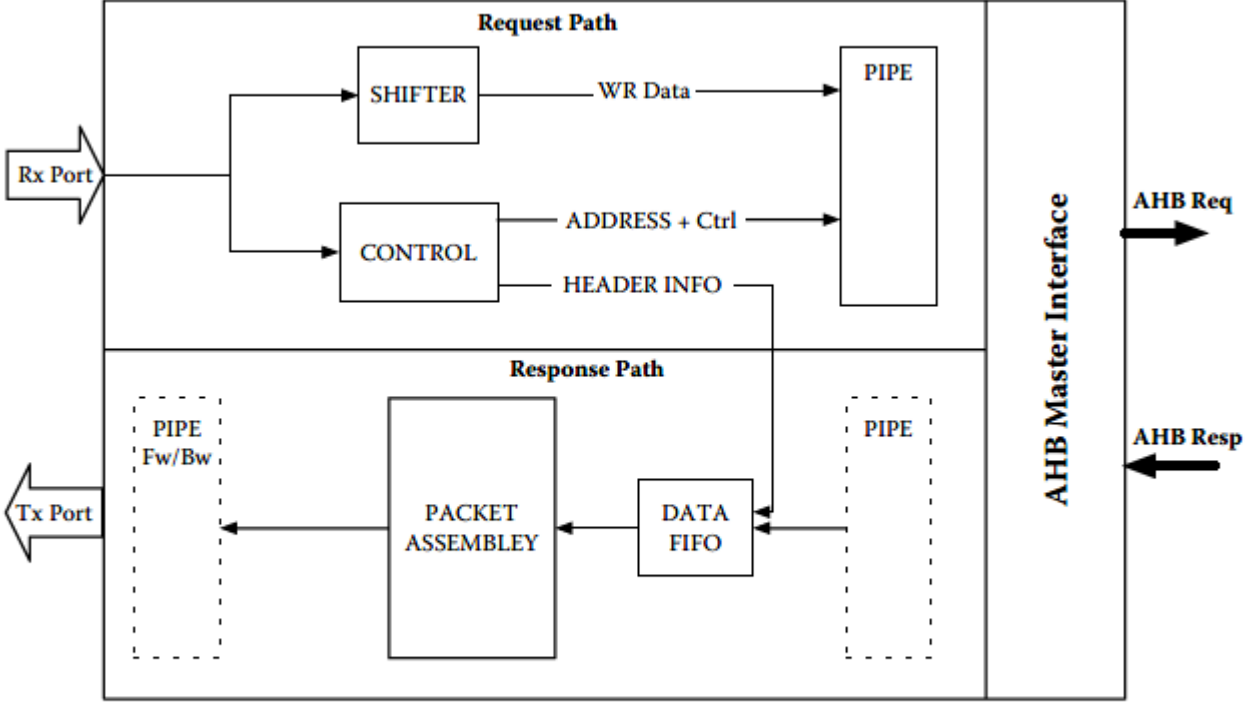
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	<p>11.3.2.2 Target NIU Units</p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always 32 bits wide, but the actual address space size may be downsized by setting a hardware parameter. Unused AHB address bits are then driven to zero. The NTTP request packet is then translated into one or more corresponding AHB accesses, depending on the transaction type (word aligned or nonaligned access). For example, if the request is an atomic Store, or a Load that can fit an AHB burst of specified length, then such a burst is generated. Otherwise, an AHB burst with unspecified length is generated.</p>

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	<p style="text-align: center;">Target NIU Architecture</p>  <p>FIGURE 11.5 Network interface unit: Target architecture.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 318-319.</p>

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	<p>In the Target NIUs of the Arteris NoC, similar to as described above for the Initiator NIUs, “[a] FIFO memory is inserted in the datapath for AHB ... accesses. The FIFO memory absorbs data at the AHB ... rate, so that NTTP packets can burst at NoC rate as soon as a minimum amount of data has been received.” “[T]he FIFO depth is defined by the hardware parameter” which “indicates the amount of data required to generate a ... packet: each time the FIFO is full, a ... packet is sent on the Tx port”:</p> <p>A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is</p> <ul style="list-style-type: none"> • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

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	<p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317-318.</p> <p>As a further illustration, the “Arteris NTTP protocol is packet-based” and the packets, which have “header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address,” are “transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes”:</p> <p>11.3.1.2 Transport Layer</p> <p>The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target.</p> <p><i>Id.</i> at 313.</p> <p>As yet a further illustration, packets in the Arteris NoC are “delivered as words that are sent along links and “[o]ne link (represented in Figure 11.1) defines the following signals,” which include “the current priority of the packet used to define preferred traffic class (or Quality of Service)” and “[f]low control”:</p>

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	<ul style="list-style-type: none"> • Data—Data word of the width specified at design-time. • Frm—When asserted high, indicates that a packet is being transmitted. • Head—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only. • TailOfs—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only. • Pres.—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2). • Vld—Data valid: when asserted high, indicates that a word is being transmitted. • RxRdy—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. <p><i>Id.</i> at 313-314.</p>

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	<p>As a further illustration, the Arteris NoC implements Quality of Service (QoS) to “provide[] a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic”; “QoS, which includes guarantees of throughput and/or latency, is achieved by exploiting the signal pressure embedded into the NTTP packet definition” where the “pressure signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed”; and the “pressure information will be embedded in the NTTP packet at the NIU level”:</p> <p>Quality of Service (QoS). The QoS is a very important feature in the inter-connect infrastructures because it provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic. Usually the end users are looking for guarantees on bandwidth and/or end-to-end communication latency. Different mechanisms and strategies have been proposed in the literature. For instance, in <i>Æthereal NoC</i> [11,24] proposed by NXP, a TDMA approach allows the specification of two traffic categories [25]: BE and GT.</p> <p>In the Arteris NoC, the QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition (Figures 11.1 and 11.2). The pressure</p>

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	<p>signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed. For example, we can imagine associating the generation of the pressure signal when a certain threshold has been reached in the FIFO of the corresponding IP. This pressure information will be embedded in the NTTP packet at the NIU level: packets that have pressure bits equal to zero will be considered without QoS; packets with a nonzero value of the pressure bit will indicate preferred traffic class.* Such a QoS mechanism offers immediate service to the most urgent inputs and variables, and fair service whenever there are multiple contending inputs of equal urgency (BE). Within switches, arbitration decisions favor preferred packets and allocate remaining bandwidth (after preferred packets are served) fairly to contending packets. When there are contending preferred packets at the same pressure level, arbitration decisions among them are also fair.</p> <p>The Arteris NoC supports the following four different traffic classes:</p>

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	<ul style="list-style-type: none"> • Real time and low latency (RTLL)—Traffic flows that require the lowest possible latency. Sometimes it is acceptable to have brief intervals of longer latency as long as the average latency is low. Care must be taken to avoid starving other traffic flows as a side effect of pursuing low latency. • Guaranteed throughput (GT)—Traffic flows that must maintain their throughput over a relatively long time interval. The actual bandwidth needed can be highly variable even over long intervals. Dynamic pressure is employed for this traffic class. • Guaranteed bandwidth (GBW)—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval. Over short periods, the network may lag or lead in providing this bandwidth. Bandwidth meters may be inserted onto links in the NoC to regulate these flows, using either of the two methods. If the flow is assigned high pressure, the meter asserts backpressure (flow control) to prevent the flow from exceeding a maximum bandwidth. Alternatively, the meter can modulate the flows pressure (priority) dynamically as needed to maintain an average bandwidth. • Best effort (BE)—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

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“Integrated circuit and method for buffering to optimize burst length in networks on chips”

'800 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip ¹
	<p data-bbox="541 282 1843 354">* Note that in the NTTP packet, the pressure field allows more then one bit, resulting in multiple levels of preferred traffic.</p> <p data-bbox="501 428 1803 500">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 315-316.</p> <p data-bbox="501 548 1885 724">In addition, the Arteris Interconnect includes “a mechanism called rated adaptation, which stalls packets just enough to remove wait states from the packets, preserving a low latency.” For other traffic, the “[b]est effort traffic can be left untouched[,]” “[l]atency sensitive traffic may have its urgency modulated as a function of the transaction[,]” “[s]oft real-time traffic may have its hurry level modulated as a function of the bandwidth it receives[,]” and “[o]n the real-time modem data port, the hurry is fixed at a critical level.”</p> <p data-bbox="512 776 1860 1032">Those effects can be mended by the insertion of buffering. In the case of peak bandwidth reduction, a simple FIFO does the job: Busy states present at the output of the FIFO do not propagate back to the input until the FIFO is full. For a peak bandwidth increase, the situation is a bit more complex. In a FIFO, wait states present at the input are only absorbed when the FIFO is not empty. Arteris proposes a mechanism called rate adaptation, which stalls packets just enough to remove wait states from the packets, preserving a low latency.</p> <p data-bbox="512 1045 1860 1166">In this second step, the architecture is modified to introduce some buffering. In our example 760 bytes of memory have been distributed across the topology. Some have been put on existing links; some required the creation of new links.</p> <p data-bbox="501 1218 1829 1328">Application driven network-on-chip architecture exploration & refinement for a complex SoC, https://www.arteris.com/hs-fs/hub/48858/file-14363521-pdf/docs/springer-appdrivennocarchitecture8.5x11.pdf, at p. 16.</p>

U.S. Patent No. 8,086,800 (Radulescu and Goossens)

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	<p>For the other traffic, the configuration can be done in architecture.</p> <ul style="list-style-type: none"> • Best effort traffic can be left untouched. • Latency sensitive traffic may have its urgency modulated as a function of the transaction: <i>Normal</i> for writes and <i>important</i> for reads. • Soft real-time traffic may have its hurry level modulated as a function of the bandwidth it receives: <i>Critical</i> until a specified bandwidth is obtained on a sliding 4 microsecond window, and <i>normal</i> thereafter. These settings are set through configuration registers and may be modified while the interconnect is running. The mechanism is called a bandwidth regulator. • On the real-time modem data port, the hurry is fixed at a critical level. <p><i>Id.</i> at 18.</p> <p>As a further illustration, the Arteris NoC implements QoS mechanisms that performs arbitration based on “Bandwidth Regularator (BR)” and “Bandwidth Limiter (BL)”:</p>

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	<h2 data-bbox="527 261 1478 326">Bandwidth Limiters and Rate Regulators</h2> <p data-bbox="527 391 1688 618">Many times architects will want to implement QoS within their SoC but the QoS prioritization data is not available from the individual IP blocks. In this case, QoS information may be generated from within the NoC interconnect using Arteris' QoS Generator. The QoS Generator can instantiate sophisticated, and software programmable, means to regulate interconnect QoS, including:</p> <ul data-bbox="575 683 1703 1000" style="list-style-type: none"> ➤ Bandwidth Limiters – Bandwidth limiters cause a socket to stop accepting requests when a run-time programmable throughput threshold has been exceeded. ➤ Rate Regulators – Rate regulators cause a socket's transactions to be demoted when a bandwidth threshold is reached. This can be considered a smoother version of the bandwidth limiter because transactions are only demoted instead of stalled. <p data-bbox="501 1024 1356 1062">https://www.arteris.com/end-to-end-quality-of-service-qos</p>